

Industry Collaborative Workshop on “VLSI Circuit Design using VHDL”
Organised by the Department of ECE
In association with IIC SurTech and Livid Design Inc.

Date and Venue: 1st November, 2025, DSCSITSC

No of Students Participated: 31

Speaker/Coordinator: Dr Arindam Sadhu and Dr pradipta Maiti

External Speaker: Mr Saurabh Kumar

Department of ECE in association with IIC SurTech and Livid Design Inc. organised a one day workshop on VLSI on 1st November, 2025. The preliminary objective was to involve the students of diploma colleges with modern technologies like design and fabrication and to inspire them for VHDL coding practice and to aware them about the current industry requirement for VLSI.

Professional trainers from Livid Design Inc. was present during the workshop. Students from different diploma colleges were participated in the workshop

Outcome of the Workshop:

Students acquired the knowledge on the following domain of IOT,

1. Introduction to Chip Design
2. VHDL Simulation Environment
3. Circuit Analysis
4. Coding Protocols
5. Design Execution

Few glimpses of the event,



The poster features a header with various institutional logos including SurTech, AICTE, NBA, UGC, NITF-Innovation, Institution's Innovation Council, and Livid Design Inc. The main title is "Industry Collaborative Workshop on 'VLSI Circuit Design using VHDL'", with a subtitle "Make Ready Yourself for VLSI Industry as Front End Designer.....". A QR code on the left is labeled "Scan for registration". A large teal box on the left contains registration details: "REGISTRATION FREE for Diploma ETCE, EE and CSE 3rd year students", "Venue : Dr. Sudhir Chandra Sur Institute of Technology and Sports Complex (540, Dumdum Road, Surer Math)", "Date : 01/11/2025, 11 am onwards", and "Organized by : Department of ECE, In Association with IIC, SURTECH & IETE-ISF, SURTECH & Livid Design INC. (Chip Design Start Up)". To the right, under the heading "Topics :", four topics are listed: "1) Basics of Logic Circuits applicable for Chip Design.", "2) Digital Logic Synthesis for Component Design in Processor Architecture.", "3) CMOS Memory design.", and "4) Hands-on Training on 'Xilinx' with Hardware Description Language (VHDL).". At the bottom, there are two more QR codes, the website "www.surtech.edu.in", and "www.jisgroup.org".

**Industry Collaborative Workshop on
“VLSI Circuit Design using VHDL”**

Make Ready Yourself for VLSI Industry as Front End Designer.....

**REGISTRATION FREE for Diploma
ETCE, EE and CSE 3rd year students**

Venue : **Dr. Sudhir Chandra Sur Institute
of Technology and Sports Complex**
(540, Dumdum Road, Surer Math)

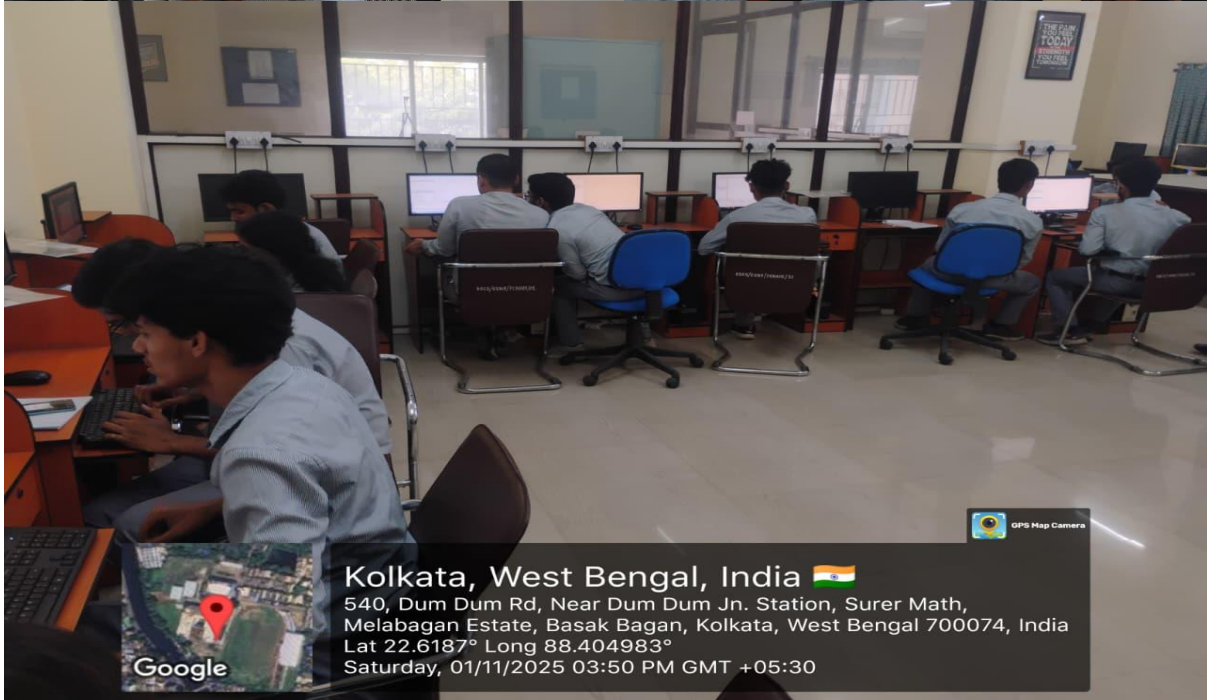
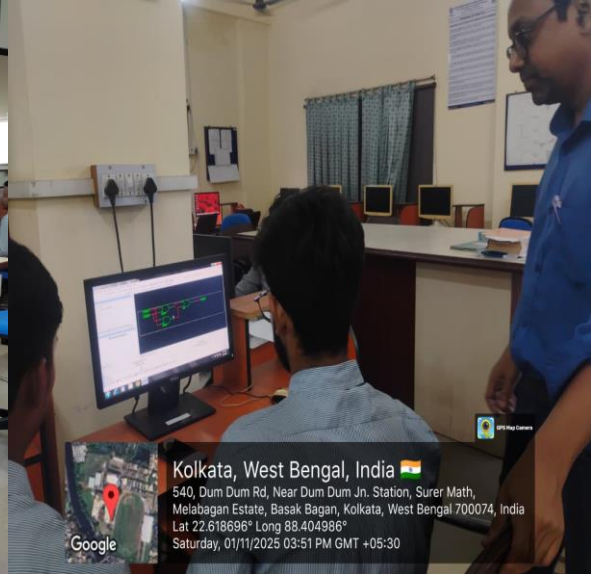
Date : **01/11/2025, 11 am onwards**

Organized by : **Department of ECE, In
Association with IIC, SURTECH & IETE-ISF,
SURTECH & Livid Design INC.**
(Chip Design Start Up)

Topics :

- 1) Basics of Logic Circuits applicable for Chip Design.
- 2) Digital Logic Synthesis for Component Design in Processor Architecture.
- 3) CMOS Memory design.
- 4) Hands-on Training on “Xilinx” with Hardware Description Language (VHDL).

www.surtech.edu.in www.jisgroup.org



Dr Anirban Neogi

HOD, ECE Department